Verification of Translation

US Patent Application No.: 09/700940

Title of the Invention: METHOD OF DISPOSING LSI

I, Yuka Moriyama, whose full post office address is IKEUCHI·SATO & PARTNER PATENT ATTORNEYS, OAP Tower 26F, 8-30 Tenmabashi, 1-chome, Kita-ku, Osaka-shi, OSAKA 530-6026, Japan am the translator of the documents attached and I state that the following is true translations to the best of my knowledge and belief of JP 11(1999)-79927 (Date of Filing: March 24, 1999).

At Osaka, Japan
DATED 06/5/2003 (Day/Month/Year)

Signature of the translator

Yuka Moriyama

Yuka MORIYAMA

PATENT OFFICE
JAPANESE GOVERNMENT

This is to certify that the annexed is a true copy of the following application as filed with this Office.

Date of Application: March 24, 1999

Application Number: Patent Application No. Heisei 11-79927

Applicant(s): Matsushita Electric Industrial Co., Ltd.

【Document Name】 Patent Application

【Case Number】 R2966

【Date of Application】 March 24, 1999

【Destination】 Director–General of the Japanese Patent Office

【Intern. Patent Classification】 H01L 27/04

【Inventor】

【Address】 c/o Matsushita Electric Industrial Co., Ltd.
1006-banchi, Oaza-Kadoma, Kadoma-shi, Osaka-fu

【Name】 Shiro SAKIYAMA

【Inventor】

【Address】 c/o Matsushita Electric Industrial Co., Ltd.
1006-banchi, Oaza-Kadoma, Kadoma-shi, Osaka-fu

【Name】 Masayoshi KINOSHITA

【Inventor】

【Address】 c/o Matsushita Electric Industrial Co., Ltd.
1006-banchi, Oaza-Kadoma, Kadoma-shi, Osaka-fu

【Name】 Jun KAJIWARA

【Inventor】

【Address】 c/o Matsushita Electric Industrial Co., Ltd.
1006-banchi, Oaza-Kadoma, Kadoma-shi, Osaka-fu

【Name】 Hiroo YAMAMOTO

【Inventor】

【Address】 c/o Matsushita Electric Industrial Co., Ltd.

1006-banchi, Oaza-Kadoma, Kadoma-shi, Osaka-fu

【Name】 Katsuji SATOMI

【Patent Applicant】

【Identification Number】 000005821

【Name/Title】 Matsushita Electric Industrial Co., Ltd.

【Attorneys】

【Identification Number】 100095555

【Patent Attorney】

【Name】 Hiroyuki IKEUCHI

【Telephone Number】 06-6361-9334

【Appointed Attorney】

【Identification Number】 100076576

【Patent Attorney】

【Name】 Kimihiro SATO

【Indication of Official Fees】

【Deposit Account Number】 012162

【Amount of Deposit】 21000

【List of File Documents】

【Name of Document】 Patent Specification 1

【Name of Document】 Drawings 1

【Name of Document】 Abstract 1

【General Power of Attorney's Number】 9003743

【Proof】 Required

[Document Name] SPECIFICATION
[TITLE OF THE INVENTION]
LSI LAYOUT METHOD
[CLAIMS]

[Claim 1] A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, comprising the operations of:

providing power supply capacitor cells as one of the standard cells,

determining a capacitance value of the power supply capacitor cells so as to correspond to a drive load capacity value of each of logic gate cells provided as one of the standard cells, and

arranging the power supply capacitor cells in the vicinity of the logic gate cells.

[Claim 2] The LSI layout method according to claim 1, wherein the capacitance value of the power supply capacitor cells is determined to be substantially twice as large as the drive load capacity value of each of the logic gate cells.

[Claim 3] The LSI layout method according to claim 1, wherein the power supply capacitor cells are arranged in the vicinity of the logic gate cells which change simultaneously with clock synchronization.

[Claim 4] A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, comprising the operations of:

providing power supply capacitor cells as one of the standard cells, and

arranging the power supply capacitor cells in spaces of each block where standard cells are not arranged by the automatic arrangement wiring.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Technical field to which the invention pertains]

This invention relates to a method for stabilizing the power supply in the LSI design using automatic arrangement wiring of standard cells.

[0002]

[Prior Art]

In the last few years, in accordance with the power increasingly consumed by LSI, LSI tends to generate increased power supply noise. Furthermore, due to the market demand to promote electric power saving, LSI with lower voltage also has been developed. With this development, an

operating margin against power supply noise in LSI internal circuits tends to be degraded.

[0003]

There is a fear that such an increase in power supply noise of LSI may have negative effects on LSI internal circuits. Examples of such negative effects are: (1) deterioration of operating speed, (2) malfunction of circuits, and (3) system malfunction caused by EMI (Electro Magnetic Interference) noise.

[0004]

For suppression of noise generated from LSI, it has been common to use a method of arranging a power supply capacity inside LSI. This is because the insertion of power supply capacity makes it possible to reduce the alternating current impedance of power supply and to suppress power supply noise caused by an alternating current power supply.

[0005]

Furthermore, JP5-21711A discloses a method for stabilizing a power supply, which is achieved by arranging the power supply capacity into sections where functional circuits of LSI do not exist. In addition, JP5-283615A discloses a method of efficiently adding power supply capacity by using capacitance between a power supply and an aluminum wire in LSI.

[0006]

[Problems to be solved by the invention]

Generally, in using CMOS (Complementary Metal-Oxide Semiconductor) integrated circuits, a charge-discharge current is generated toward load capacity when switching takes place. FIG. 9 illustrates a circuit diagram of a general CMOS integrated circuit. FIG. 9 illustrates a PMOS (P-channel MOS) transistor switch 91, a NMOS (N-channel MOS) transistor switch 92, a ground electrode 93, a power supply capacitor 94, a load capacitor 95, a power supply (Vdd) pad 96, a power supply (Vss) pad 97, a charge current 98, and a parasitic inductor 99.

[0007]

With reference to FIG. 9, when the PMOS (P-channel MOS) transistor switch 91 is turned on, the charge current 98 (Ivdd) flows from the power supply to the load capacitor 95. When the NMOS (N-channel MOS) transistor switch 92 is turned on, a discharge current to the ground electrode 93 is generated.

[0008]

The power supply capacitor 94 has accumulated charge energy. The arrangement of the power supply capacitor 94 into the CMOS integrated circuit makes it possible to provide an electric current (Ic) also from the power supply capacitor 94 in addition to the electric current (Ivdd) supplied from the power supply pad 96. Therefore, the variation of current supply from the power supply (Vdd) pad 96 can be controlled.

[0009]

However, with the increased development of miniature semiconductor integrated circuits in the last few years, the use of an inductor element (L) of an aluminum wire inside LSI tends to increase. Moreover, in using a general CMOS circuit, the parasitic inductor 99 is generated, and this causes power supply noise. More specifically, the power supply noise (ΔV) can be expressed as:

$$\Delta V = L \times di / dt \qquad \text{(Formula 1)}$$

In the formula 1, di / dt represents a variation of electric current. It is clear from Formula 1 that an effective approach for reduction of power supply noise (ΔV) is either to reduce the variation of electric current (di / dt) or to reduce the parasitic inductor element L. In other words, the parasitic inductor element L increases in proportion to the length of the aluminum wire, so that it is effective to shorten the power supply line on which a current change takes place.

[0010]

However, in the conventional method described above, the aluminum wire extending from the switched CMOS gate circuit to the power supply capacity was relatively long, so that the power supply inductor element from the power supply capacity to the switching circuit was increased largely. Therefore, it was difficult to achieve sufficient effectiveness for reduction of power supply noise.

[0011]

In order to solve the above mentioned problems, it is an object of the present invention to provide a LSI layout method for the LSI design of standard cell type, by which sufficient noise suppression as well as sufficient stabilization of the power supply can be achieved.

[0012]

[Means for solving problems]

To achieve this purpose, the present invention provides a LSI layout method for the LSI design by automatic arrangement wiring of standard

cells, characterized in that power supply capacitor cells are provided as one of the standard cells, a capacitance value of the power supply capacitor cells is determined so as to correspond to a drive load capacity value of each of logic gate cells provided as one of the standard cells, and the power supply capacitor cells are arranged in the vicinity of the logic gate cells.

[0013]

According to this configuration, the power supply capacitor cells are arranged in the vicinity of the logic gate cells with optimal capacitance values corresponding to the load capacity of the logic gate cells. Thus, noise caused by parasitic inductors can be prevented from increasing, and the power supply noise element can be reduced.

[0014]

Additionally, in the LSI layout method of the present invention, the capacitance value of the power supply capacitor cells is preferably determined to be substantially twice as large as the drive load capacity value of the logic gate cells. If the capacitance value is determined to be about twice as large as the total load capacity of the logic gate standard cells, the power supply noise can be suppressed to about 1/10 or less of the power supply voltage.

[0015]

Moreover, in the LSI layout method of the present invention, the power supply capacitor cells preferably are arranged in the vicinity of the logic gate cells, which change simultaneously with clock synchronization. By arranging the power supply capacitor cells in the vicinity of the clock-synchronous logic gates, an area loss can be minimized and the power supply noise can be suppressed efficiently.

[0016]

Next, to achieve this purpose, the present invention provides a LSI layout method for the LSI design using automatic arrangement wiring of standard cells, characterized in that power supply capacitor cells are provided as one of the standard cells, and that the power supply capacitor cells are arranged in spaces of each block where standard cells are not arranged by automatic arrangement wiring.

[0017]

According to this configuration, the power supply capacitor is arranged in spaces of each circuit block where standard cells are not arranged (dead space). Thus, the output impedance of power supply can be

reduced without increasing the block area, and the power supply noise can be reduced.

[0018]

[Mode for carrying out the invention]

Embodiment 1

Hereinafter, a first embodiment of the LSI layout method of the present invention will be described with reference to the accompanying drawings. FIG. 1 is a general LSI block diagram; FIG. 2 is a wiring diagram of Block A formed by automatic arrangement wiring; and FIG. 3 is a wiring diagram formed by automatic arrangement wiring, provided with power supply capacitor cells according to the first embodiment of the LSI layout method of the present invention.

[0019]

FIG. 1 illustrates LSI 1 and circuit blocks 11 to 13 in a block layout using standard cells. As illustrated in FIG. 2, each block is composed of standard cells, and each block is arranged in a rectangular form. The present invention is characterized in that standard cells 22 composed of merely power supply capacitors are prepared in advance as standard cells. The power supply capacitor standard cells 22 are arranged in accordance with the load capacity of each logic gate standard cell 21, as illustrated in FIG. 3, in the vicinity of logic gate standard cells 21.

[0020]

Since the power supply capacitor standard cells 22 are arranged in the vicinity of the logic gate standard cells 21, a charge current toward a load capacity generated when each logic gate standard cell is switching can be provided for the most part from the power supply capacitor placed in the vicinity, so that the power supply noise indicated as the power supply inductor element L in Formula 1 can be reduced.

[0021]

It is generally known that if power supply noise (ΔV) is determined to be about twice as large as the total load capacity of the logic gate standard cells 21, ΔV can be suppressed to about 1/10 or less of the power supply voltage (Vdd). (P. Larsson, "di/dt Noise in CMOS Integrated Circuits.", Analog Integrated Circuits and Processing, An International Journal Vol. 14, pp.113-129, 1997.)

Furthermore, the fact that the noise is 1/10 or less of the power supply voltage means that, seen from another perspective, the noise

corresponds to about 1/2 of the voltage value of a CMOS threshold voltage. Thus, the suppression of the power supply noise to 1/2 of the threshold voltage becomes a particularly significant element for securing reliability in LSI operations.

[0022]

Specifically, as illustrated in FIG. 4 as a cell composition of standard cell type, at the time when an automatic arrangement is executed, drive load capacity of each logic gate (C1+C2) is estimated, and a power supply capacitor standard cell 21 having power supply capacity Cd of at least twice as much as the drive load capacity of each logic gate is placed in the vicinity of each logic gate. In other words, the power supply capacitor standard cell 21 is placed so as to satisfy $Cd > 2 (C1+C2)$. This arrangement assures that the power supply noise (ΔV) can be suppressed to at least 1/10 of the power supply voltage in the respective logic gate circuit. As a result, the peak value of the power supply noise in the LSI as a whole can be certified.

[0023]

As for the structure of the power supply capacitor, an optimal configuration in a CMOS semiconductor integrated circuit is illustrated in FIG. 5. More specifically, in a p-sub wafer, a n-well is fixed to Vss and a polysilicon gate electrode is fixed to Vdd. The potential of the gate electrode is determined to be forward bias against the n-well, so that depletion layer capacitance is not produced. Therefore, in spite of its small area, a power supply capacitor having a large capacitance value can be realized.

[0024]

On the other hand, the arrangement of the power supply capacitor standard cells 22 to all the logic gates creates a large area loss. Furthermore, the power supply noise reaches its peak value when a plurality of logic gates switch simultaneously. Generally, in LSI which operates according to a complete clock-synchronous pattern, a large number of logic gates switch when the clock starts. This is because all the DFF (D Flip-Flop) are designed to operate at the start of the clock. Moreover, with the acceleration of LSI in recent years, the reduction of clock skew is desired.

[0025]

With the foregoing background in mind, a design technique called CTS (Clock tree Synthesis) is more and more standardized. This method is

one of those methods that can adjust timing so that phases of all the DFF operations become the same. This timing adjustment can be executed by inverter delays in view of wiring delays. FIG. 6 illustrates a typical example of a LSI design using the CTS method. In FIG. 6, DFF standard cells 23 and inverter standard cells 24 are illustrated. The clock phases of all the DFF standard cells can be adjusted to become the same by changing the size etc. of the inverter according to the load capacity, or by adjusting the number of stage of the inverter delays and so forth.

[0026]

As a result of the high precision achieved by the CTS method, all the DFF now execute switching simultaneously. The problem of power supply noise is most crucial in such a case. Therefore, in view of the balance to be attained between the area reduction of LSI as a whole and the noise suppression effects, the most effective way is to use the above CTS method only for synchronous type logic gates (DFF gates or inverter gates used for CTS etc.) in arranging the power supply capacitor standard cells 22.

[0027]

According to the first embodiment described above, power supply capacitor cells are newly prepared in the conventional LSI layout method using standard cells, and the power supply capacitor cells with an optimal capacitance value corresponding to the load capacity of logic gate cells are arranged in the vicinity of the logic gate cells. As a result, power supply noise caused by parasitic inductors can be prevented from increasing, and the power supply noise element can be reduced. Furthermore, when the above method is applied only to clock-synchronous type logic gates, the area loss can be kept to a minimum, and the power supply noise can be suppressed efficiently.

[0028]

Embodiment 2

Next, a second embodiment of the LSI layout method of the present invention will be described with reference to the accompanying drawings. FIG. 7 is a block layout formed by automatic arrangement wiring using conventional standard cells. As illustrated in FIG. 7, the conventional configuration allows dead spaces 71 to exist, which are empty spaces in blocks where standard cells are not arranged. This is due to the following reason. Each block is composed of a plurality of power supply lines on which standard cells are arranged. Since each power supply line is

provided with a different number of standard cells, the width of the block in each power supply line differs accordingly, producing these dead spaces. In the second embodiment, as illustrated in FIG. 8, the power supply capacitor standard cells 22 are arranged in these dead spaces 71. Accordingly, the power supply capacitor cells can be arranged efficiently without changing the conventional configuration of the block 11 and the total block area.

[0029]

Generally, as the power supply capacitor becomes larger, the output impedance of the power supply is reduced. Therefore, to suppress power supply noise effectively, it is advantageous to arrange as many power supply capacitor cells as possible. On the other hand, the block area is physically limited. The second embodiment makes it possible to add power supply capacitor cells without enlarging the total block area. This embodiment can be realized easily by preparing the power supply capacitor cells 22 as standard cells, calculating the possible number of the power supply capacitor cells 22 to be arranged based on the width of the dead spaces of the power supply and the width of the power supply capacitor cells 22, and arranging as many power supply capacitor cells 22 as possible.

[0030]

According to the second embodiment described above, the power supply capacitor cells 22 are newly prepared, and the power supply capacitor cells 22 are arranged as much as possible in the dead spaces 71, which always existed in each circuit block when automatic arrangement wiring was executed by the conventional method. As a result, the output impedance of power supply can be reduced without enlarging the total block area, and the power supply noise can be reduced effectively.

[0031]

Semiconductor integrated circuits designed with the use of this method have the advantages of generating less power supply noise and preventing malfunction of circuits from occurring and so forth. Therefore, by applying this semiconductor integrated circuit to various systems and devices, systems and devices with improved quality can be provided.

[0032]

Moreover, the embodiments described above are only examples of the present invention and do not limit the present invention thereto. The subject matter of the present invention is only limited by claims.

[0033]

[Effects of the invention]

According to the LSI layout method of the present invention described above, in the conventional LSI design using standard cells, power supply capacitor cells with an optimal capacitance value corresponding to the load capacity of logic gate cells are arranged in the vicinity of the logic gate cells. Thus, compared with the conventional LSI layout method, the L-Element of wires in the power supply can be reduced, so that the power supply noise can be suppressed effectively.

[0034]

Furthermore, the LSI layout method of the present invention is applied only to logic gates of clock-synchronous type, so that the area loss can be kept to a minimum, and the power supply noise can be suppressed efficiently.

[0035]

In addition, according to the LSI layout method of the present invention, power supply capacitor cells are arranged in dead spaces which were already available in each circuit block. This configuration enables the reduction of output impedance of power supply without enlarging the total block area and also the reduction of power supply noise.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[FIG. 1] FIG. 1 is a block diagram of LSI.

[FIG. 2] FIG. 2 is a wiring diagram of a block formed by automatic arrangement wiring.

[FIG. 3] FIG. 3 is a wiring diagram formed by automatic arrangement wiring, provided with power supply capacitor cells in Embodiment 1 of the LSI layout method of the present invention.

[FIG. 4] FIG. 4 is a diagram for explanation of deciding the optimal power supply capacity in Embodiment 1 of the LSI layout method of the present invention.

[FIG. 5] FIG. 5 is an illustrative view of a power supply capacitor in a CMOS semiconductor integrated circuit.

[FIG. 6] FIG. 6 is an illustrative view of a CTS designed circuit.

[FIG. 7] FIG. 7 is an illustrative view of a block layout formed by automatic arrangement wiring using conventional standard cells.

[FIG. 8] FIG. 8 is an illustrative view of a block layout formed by automatic arrangement wiring using standard cells in Embodiment 2 of the LSI layout method of the present invention.

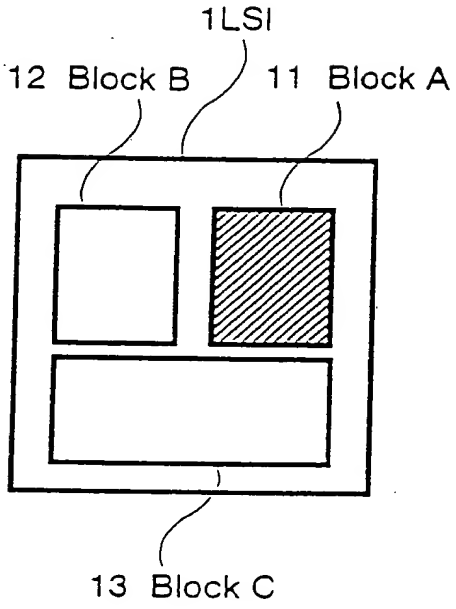
[FIG. 9] FIG. 9 is a block diagram of a conventional CMOS integrated circuit.

[Explanation of letters or numerals]

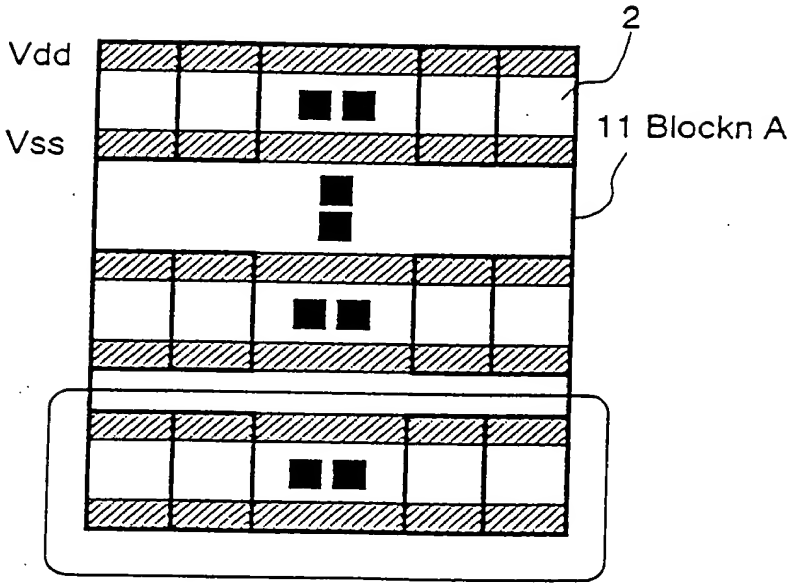
1	LSI
11,12,13	circuit block
2	standard cell
21	logic gate standard cell
22	supply capacitor standard cell
23	DFF standard cell
24	inverter standard cell
41	load capacity C1
42	load capacity C2
43	power supply capacity Cd
71	dead space
91	PMOS transistor switch
92	NMOS transistor switch
93	ground electrode
94	power supply capacitor
95	load capacitor
96	power supply (Vdd) pad
97	power supply (Vss) pad
98	charge current
99	parasitic inductor

[Document Name] Drawings

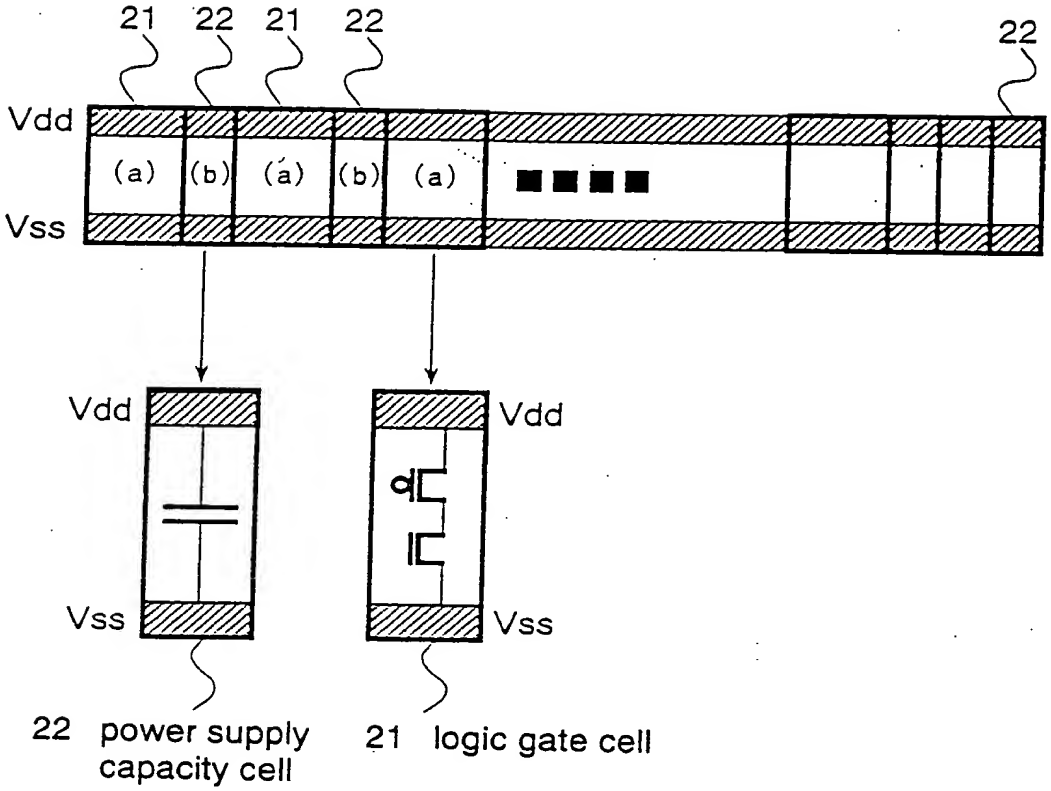
[FIG. 1]



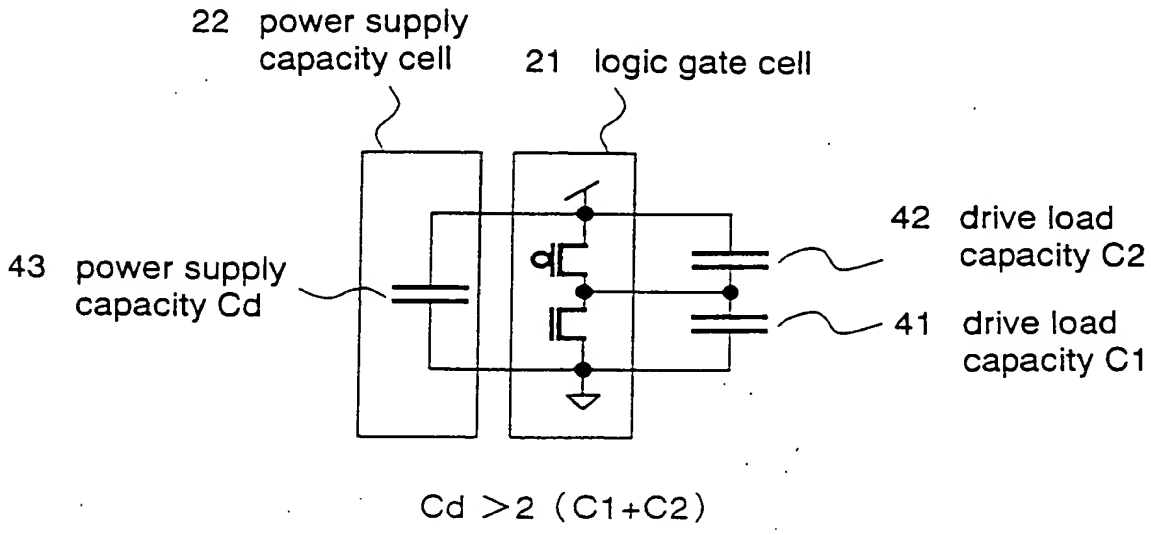
[FIG. 2]



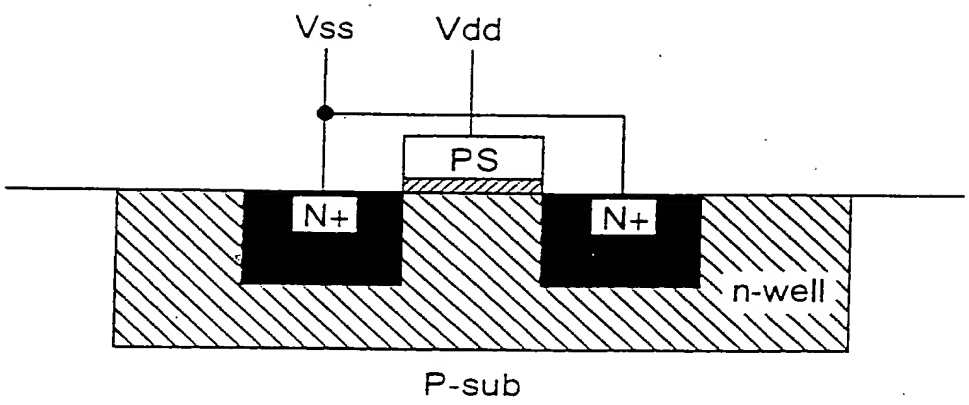
[FIG. 3]


21
22
21
22
22
Vdd
(a)
(b)
(a)
(b)
(a)
Vss
Vdd
Vdd
Vss
Vss
22 power supply capacity cell
21 logic gate cell

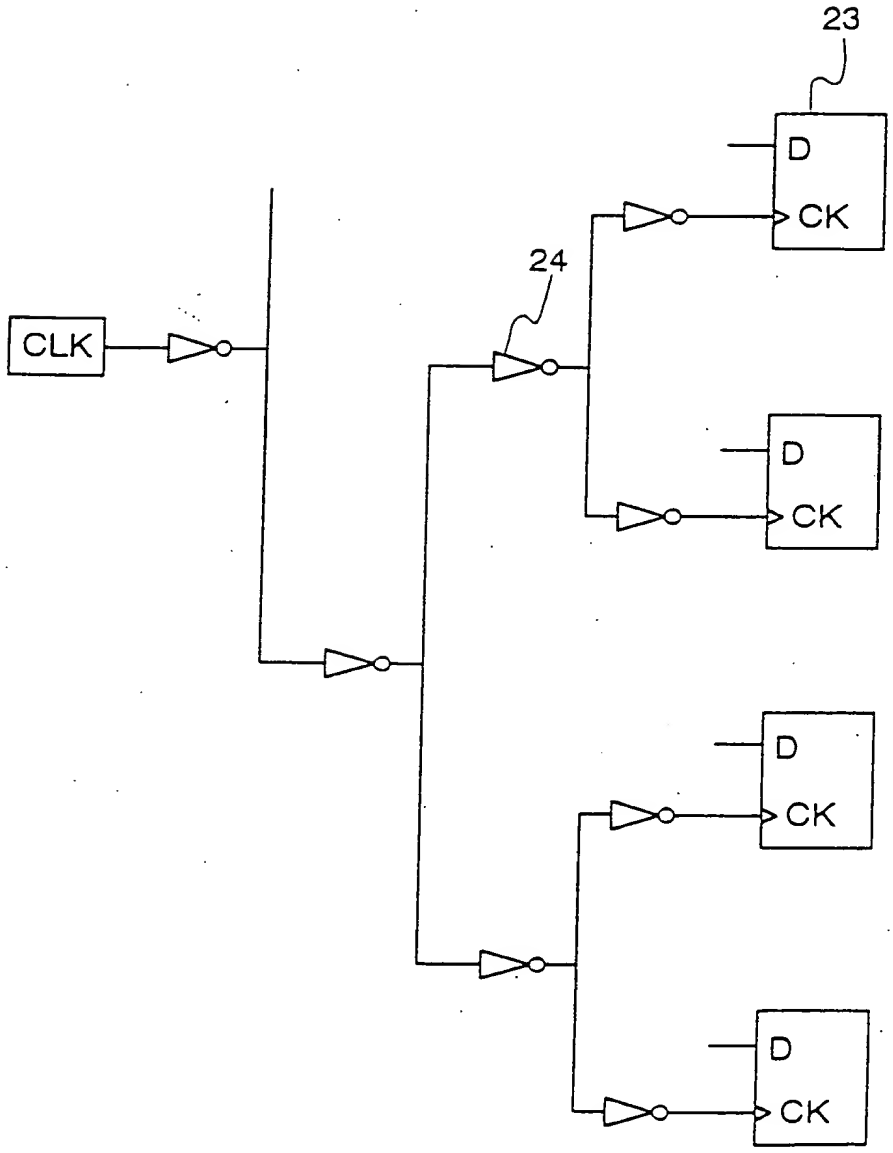
[FIG. 4]


22 power supply capacity cell
21 logic gate cell
43 power supply capacity Cd
42 drive load capacity C2
41 drive load capacity C1
Cd >2 (C1+C2)

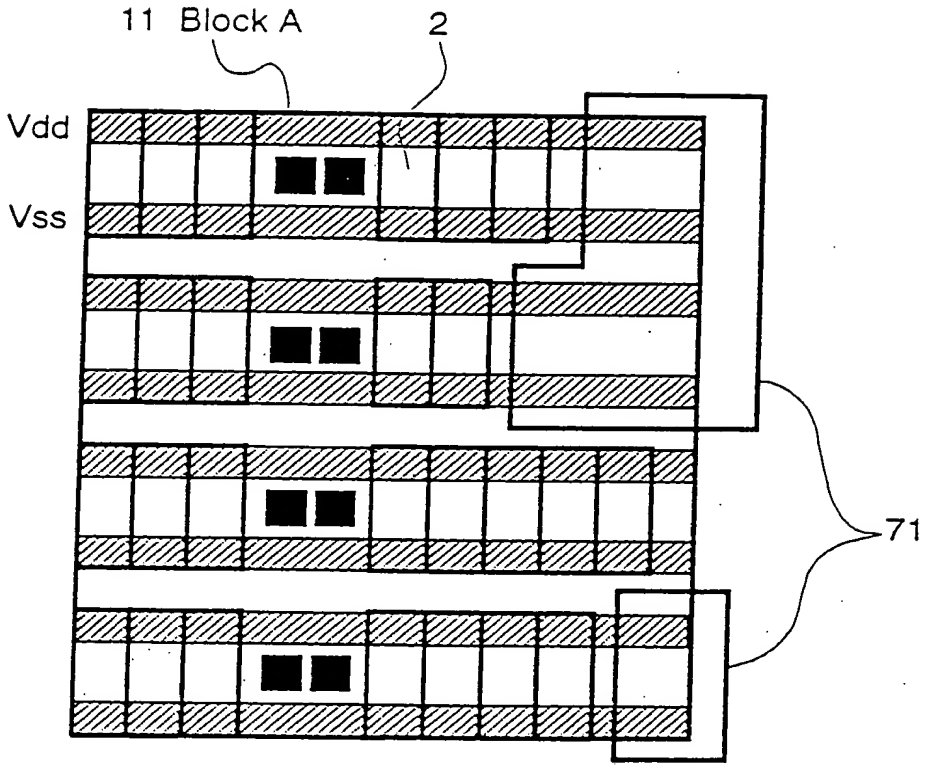
[FIG. 5]



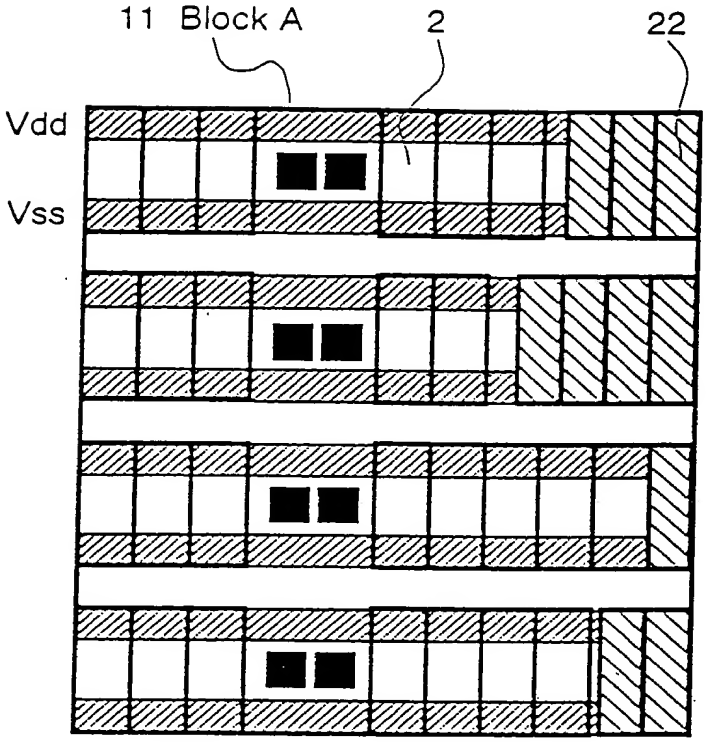
[FIG. 6]



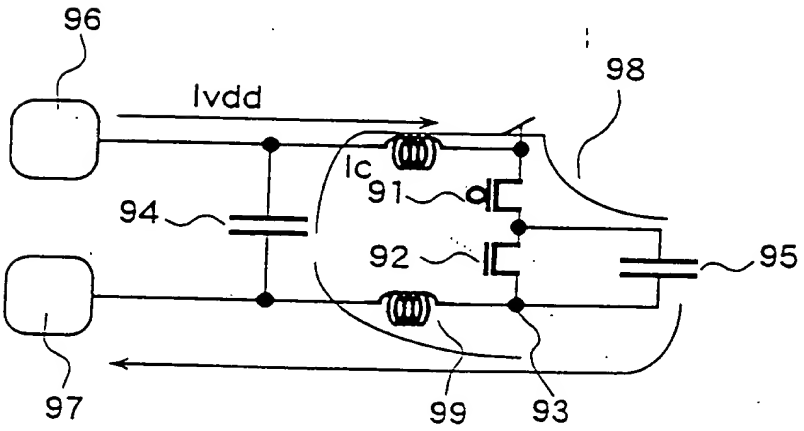
[FIG. 7]



[FIG. 8]



[FIG. 9]



[Document Name] ABSTRACT

[Abstract]

[Object] A LSI layout method for the LSI design of standard cell type is provided, by which sufficient noise suppression of power supply noise as well as sufficient stabilization of power supply can be realized.

[Means to Solve the Problems] In a LSI layout method for the LSI design of standard cell type, power supply capacitor cells are provided as one of the standard cells in addition to logic gate cells provided as one of the standard cells. Next, the capacitance value of the power supply capacitor cells is determined so as to correspond to the drive load capacity value of the logic gate cells, and the power supply capacitor cells are arranged in the vicinity of the respective logic gate cells.

[Selected Figure] FIG. 3